

Fabrication and characterization of 16x16 analog memristor 1R crossbar arrays

M. Horský¹, S. Krylov¹, N. K. Calvo¹, M. Dehghan¹, R. Stoklas¹, T. Izsák¹, M. Precner¹, T. Ščepka¹, J. Dzuba², B. Hudec^{1*}

¹Institute of Electrical Engineering, Slovak Academy of Sciences, Bratislava, Slovakia

²Bizzcom s.r.o., Bučany, Slovakia

*boris.hudec@savba.sk

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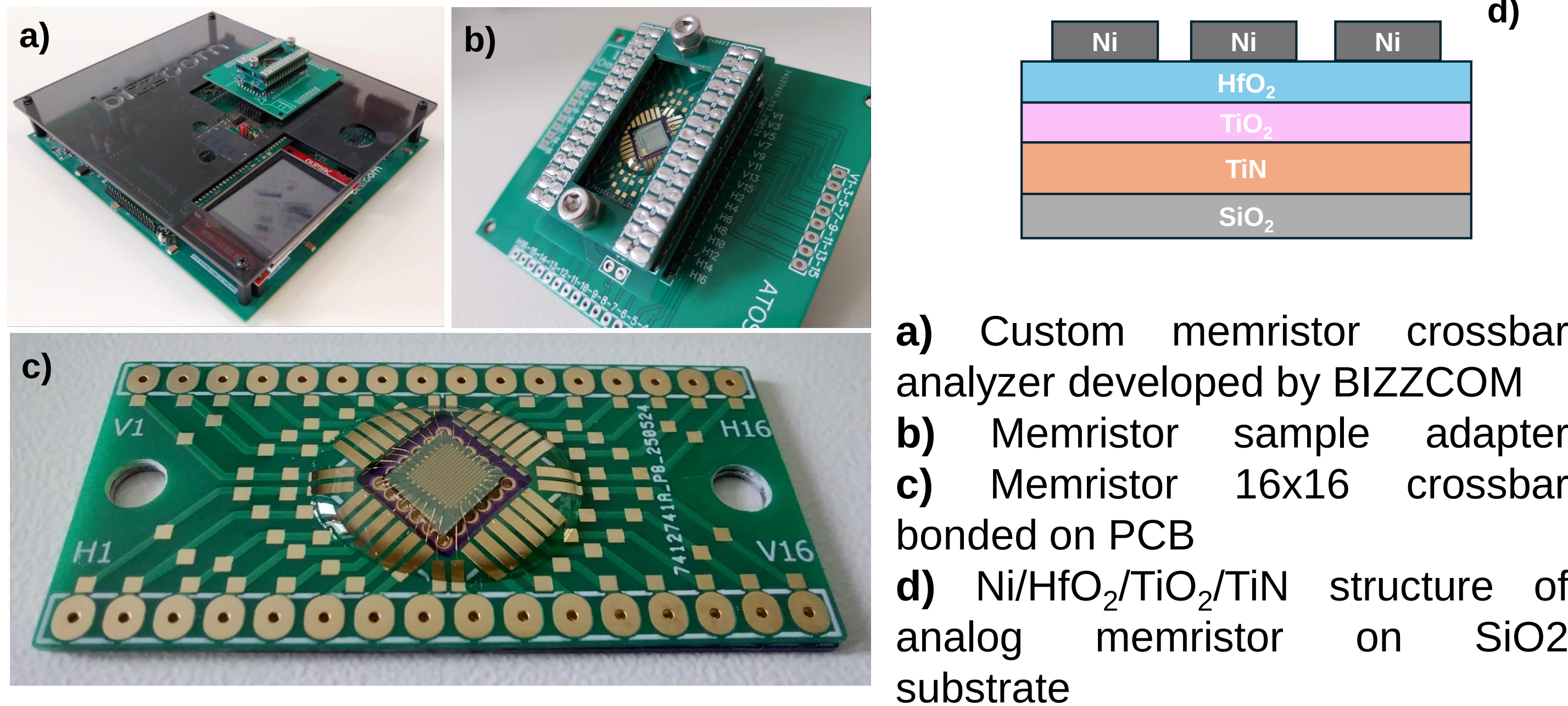


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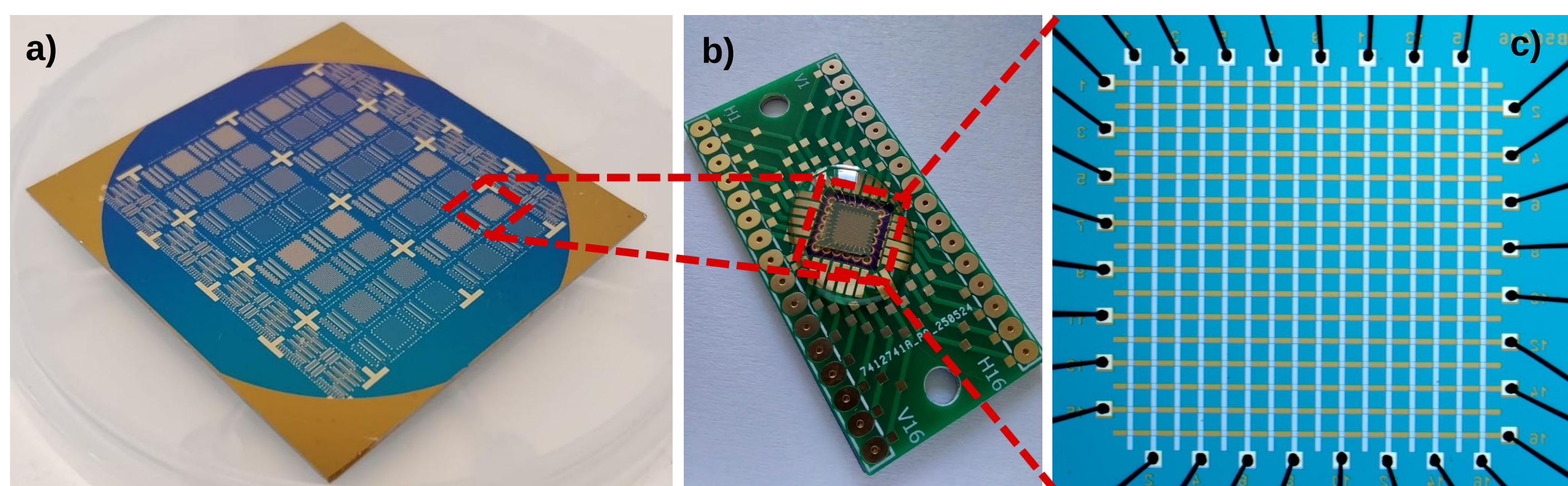
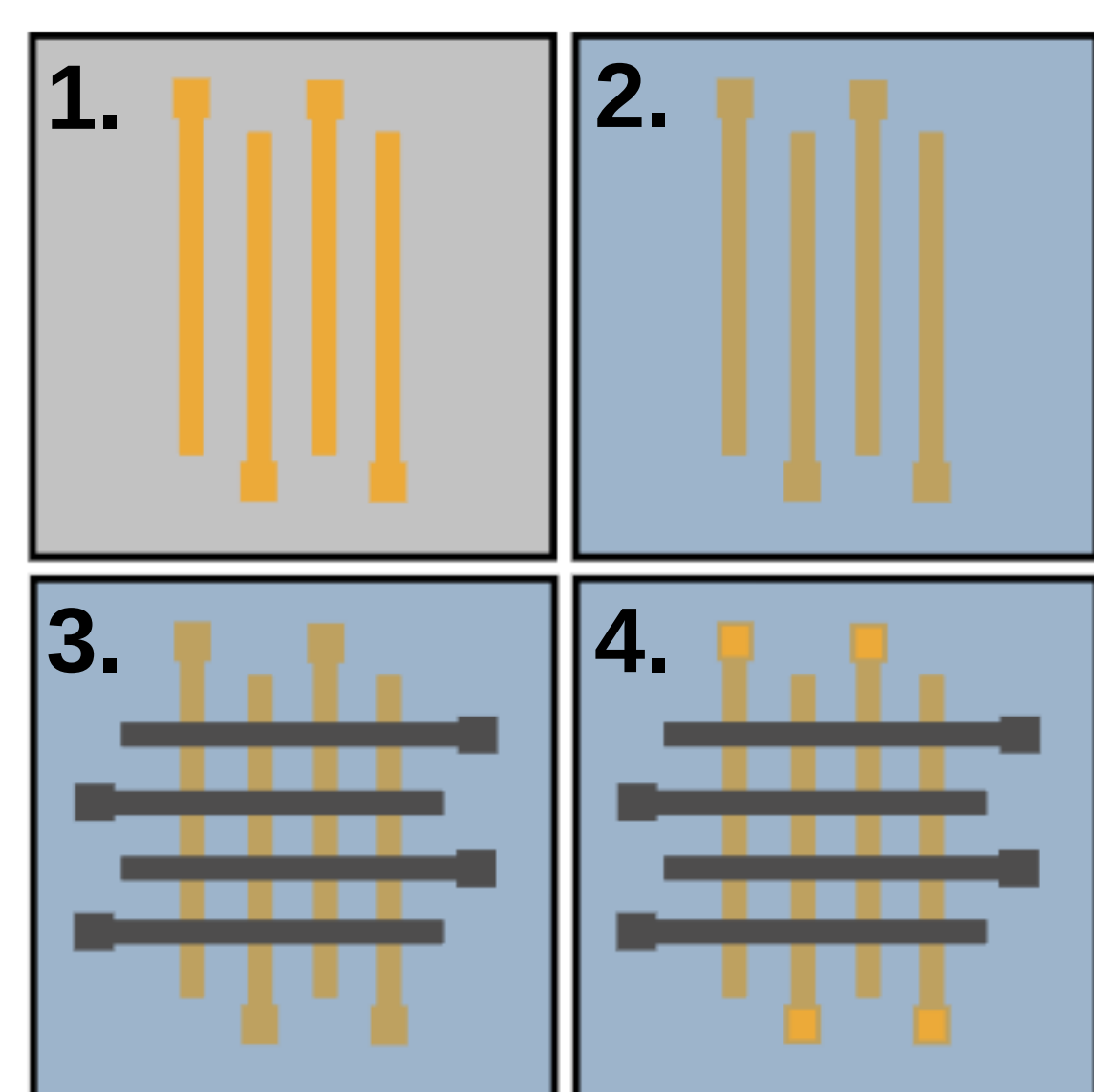
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Introduction

With the rise of neuromorphic and edge-computing applications, memristors have become essential building blocks for compact, efficient hardware. We investigate Ni/HfO₂/TiO₂/TiN analog memristors crossbars and their potential to suppress sneak path currents in crossbar arrays without additional selector devices.



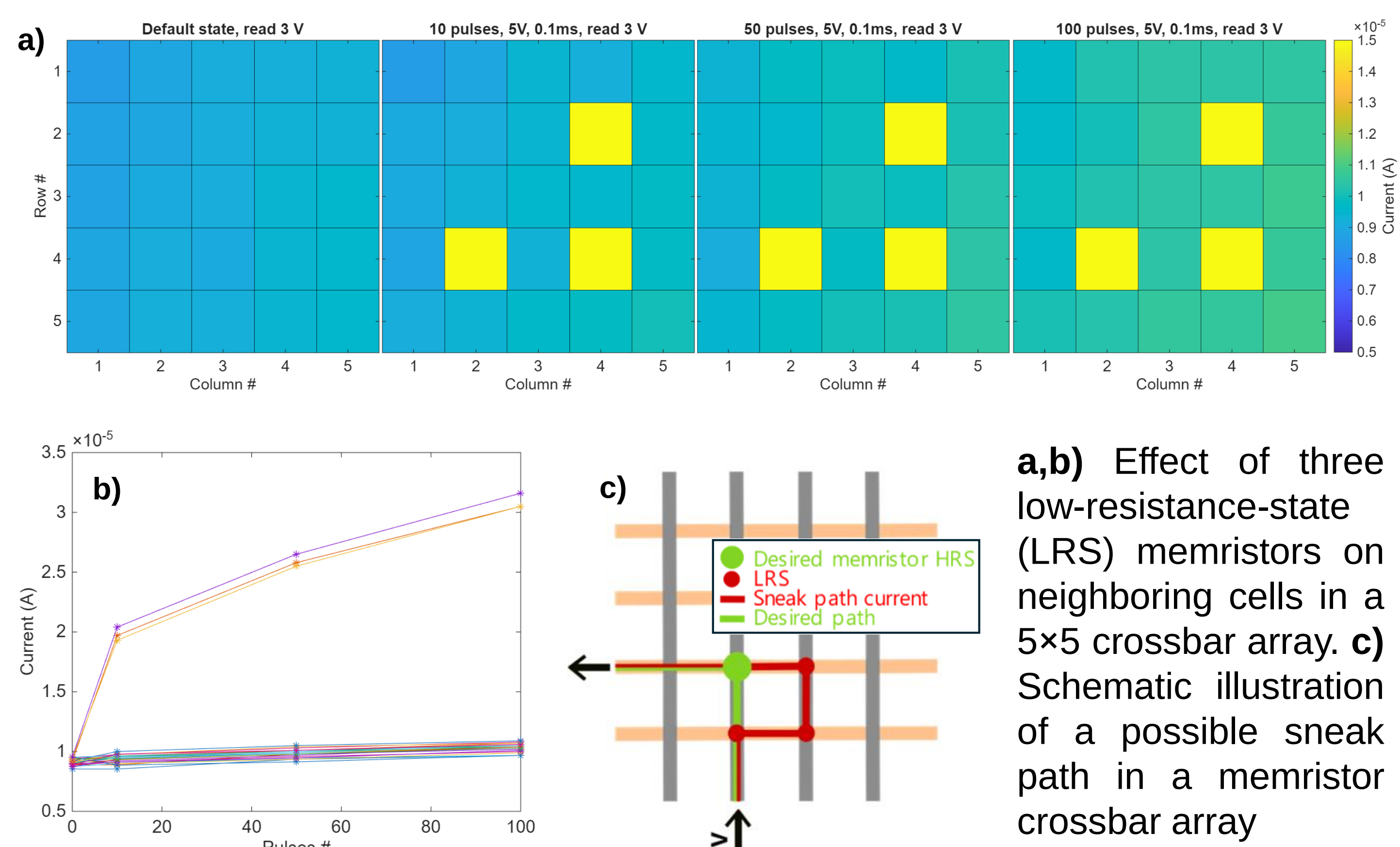
a) Custom memristor crossbar analyzer developed by BIZZCOM
b) Memristor sample adapter
c) Memristor 16x16 crossbar bonded on PCB
d) Ni/HfO₂/TiO₂/TiN structure of analog memristor on SiO₂ substrate



a) Final sample with 32 16x16 memristor arrays, b) Bonded 16x16 sample on PCB, c) bonded 16x16 crossbar of analog memristors

1. Deposition of TiN (PVD) + photolithography + etching TiN for bottom electrodes
2. ALD deposition of TiO₂ + HfO₂
3. Photolithography + deposition of Ni top electrode
4. Etching of TiO₂ + HfO₂ for bottom TiN contacts

Sneak-path current



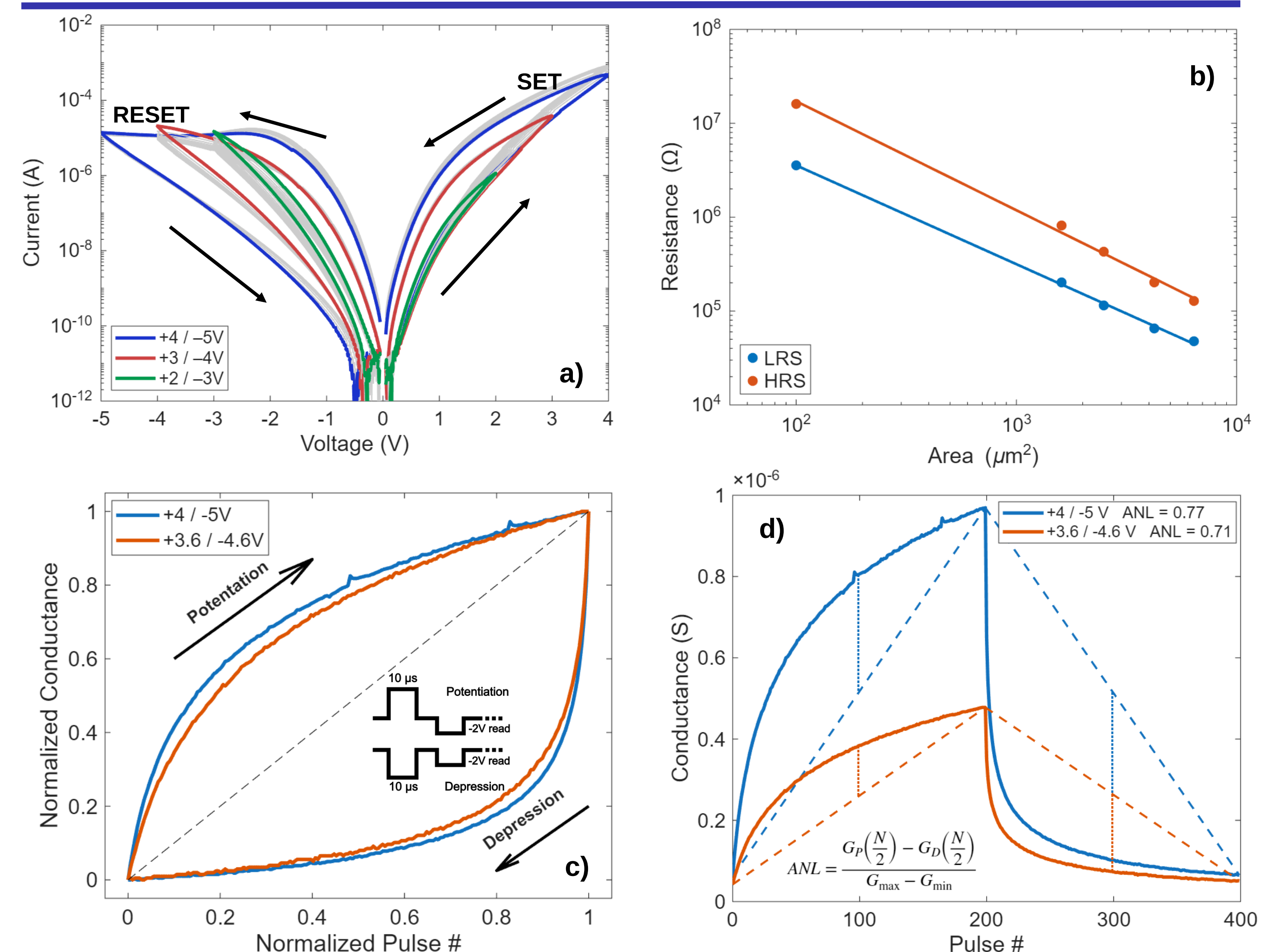
a,b) Effect of three low-resistance-state (LRS) memristors on neighboring cells in a 5x5 crossbar array. c) Schematic illustration of a possible sneak path in a memristor crossbar array

A major obstacle in memristor crossbar development is the **sneak-path current**, which causes interference between neighboring memristors and may result in misinterpretation that influences the operation of memristor crossbar arrays [1]

References

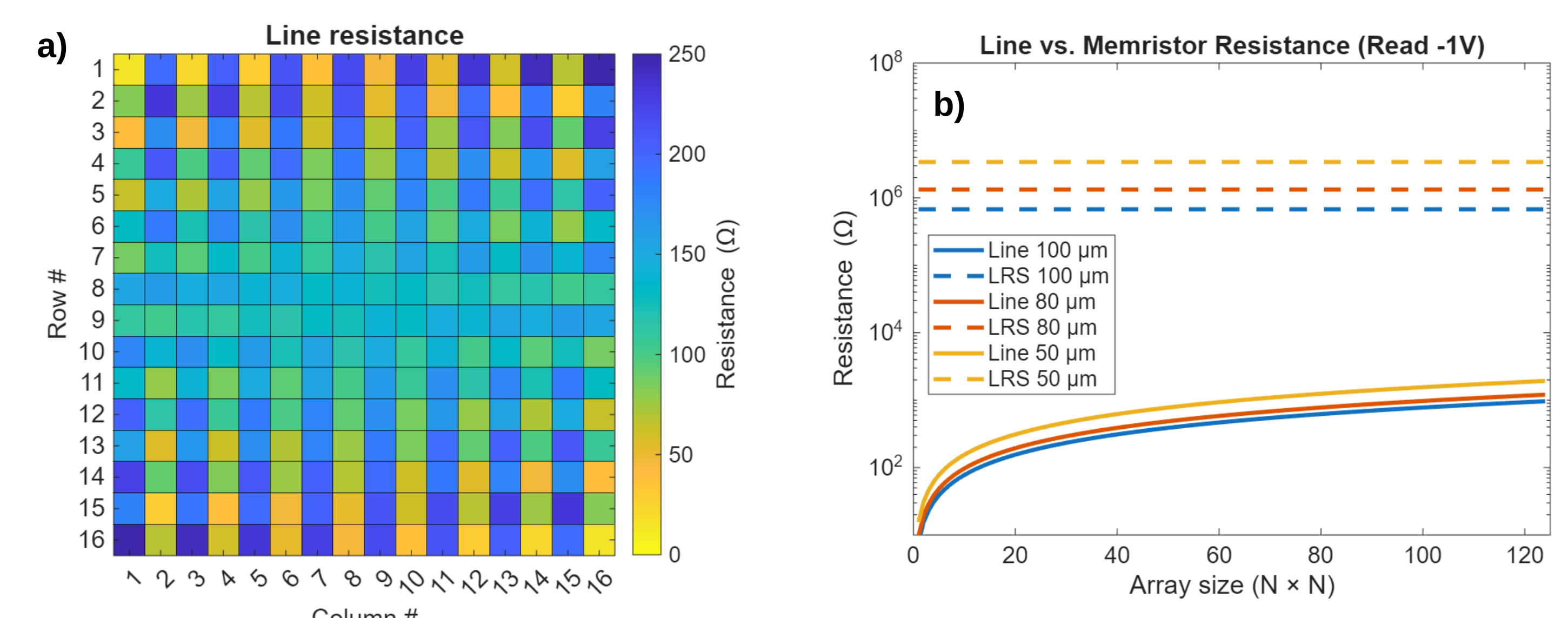
- [1] Shi *et al.*, "Research Progress of the Solutions to the Sneak Path Issue in Memristor Crossbar Arrays," *Nanoscale Adv.*, vol. 2, pp. 1824–1847, 2020, doi: 10.1039/D0NA00100G
- [2] N. Upadhyay *et al.*, "Engineering Tunneling Selector to Achieve High Non-linearity for 1S1R Integration," *Front. Nanotechnol.*, vol. 3, 2021, doi: 10.3389/fnano.2021.656026

Measurements



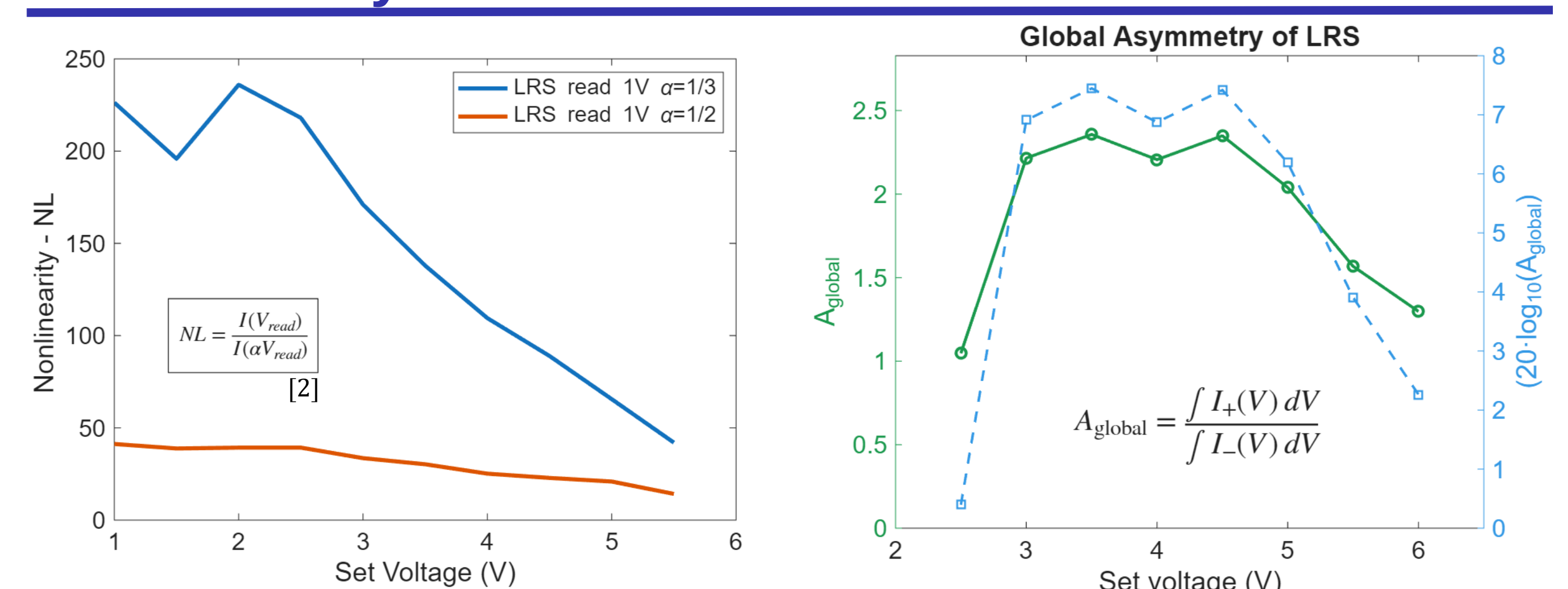
a) I-V characteristics b) Resistance of analog memristors scales with the top electrode area. c) Normalized potentiation and depression (PD) measurement, the dashed line represents the ideal behavior d) PD measurement results.

Line-resistance



a) Heat map of the line resistance for each memristor in the crossbar b) Line resistance of the longest-connected memristor based on array size, compared with the memristor's LRS

Non-linearity



Summary

- Line resistance is much smaller than memristor resistance and remains negligible even for large (120x120) arrays.
- No sneak-path effects were observed during programming, thanks to the memristor's nonlinear I-V behavior.
- These results demonstrate that the developed devices are well-suited for 1R (selector-less) memristor crossbar architectures

Acknowledgements

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